Library

Bharatiya Vidya Bhavan's

Sardar Patel College of Engineering

(A Government Aided Autonomous Institute)

Munshi Nagar, Andheri (West), Mumbai – 400058.

End Sem Re - Exam

June 2017

Q. P. Code:

Max. Marks: 100

Duration: 3 **hr**

Class: **Third Year** Semester: **VI**

Program: **Electrical Engineering**

MASTER FILE

Name of the Course: **Elective – VLSI**

Course Code : BTE332

Instructions:

- Question One is Compulsory.
- Solve any four of remaining six questions.
- Illustrate your answers with neat sketches wherever necessary.
- Assume suitable data if required.
- Preferably, write the answers in sequential order.

Question No.			Module Number	Course Outcome	Max. Marks
Q1.					
	A)	Compare the two technology scaling methods, namely, (i) the constant electric-field scaling and (ii) the constant power-supply voltage scaling. In particular, show analytically by using equations how the delay time, power dissipation, and power density are affected in terms of the scaling factor, S.	1	1	5
	B)	Compare BJT, NMOS and CMOS technology.	1	1	5
	C)	Explain simplified process sequence for the fabrication of the n-well CMOS integrated circuit with a single	1	1	5

polysilicon layer, showing only major fabrication steps.

D) Consider a simple abrupt pn-junction, which is reverse-biased with a voltage V_{bias}. The doping density of the n-type region is $N_D = 10^{19}$ cm^{-3}, and the doping density of the p-type region is given as $N_A = 10^{16}$ cm^{-3} The junction area is A = 20 μm x 20 μm. **1 1 5**

I) Find built in junction capacitance.

II) Calculate the Zero bias junction capacitance.

Given:

$\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm, $\varepsilon_{si} = 11.7 * \varepsilon_0$

$q = 1.6 \times 10^{-19}$C, $k = 1.3 \times 10^{-23}$ J/K

Intrinsic carrier concentration of silicon (Si) ni = 1.45×10^{10} (cm^{-3}) at 300K.

Thermal voltage kT/q = 0.026 V.

Q2.

A) Give the CMOS inverter voltage transfer characteristics and operating regions. **2 2 5**

B) Design a resistive-load inverter with R = 1 kΩ, such that V_{OL} = 0.6 V. The nMOS driver transistor has the following parameters: **2 2 5**

$V_{DD} = 5.0$ V

$V_{T0} = 1$ V

$\gamma = 0.2$ V$^{1/2}$

$\lambda = 0$

$\mu_n C_{ox} = 22.0$ μA/V^2

(a) Determine the required aspect ratio, W/L.

(b) Determine V_{IL} and V_{IH}.

(c) Determine noise margins N_{ML} and N_{MH}.

C) Consider a CMOS inverter circuit with the following parameters: **2 2 10**

$V_{DD} = 5$V

$V_{T0,n} = 0.6$ V

$V_{TO,p} = -0.7$ V

$k_n = 100$ μA/V^2

$k_p = 40$ μA/V^2

Calculate the noise margins of the circuit. Notice that the CMOS inverter being considered here has $k_R = 2.5$ and $V_{T0,n} \neq |V_{T0,P}|$ hence, it is not a symmetric inverter.

Q.3				
A)	Draw the circuit and layout of CMOS NAND2 gate.	2	2	5
B)	Define: i) Pseudo-nMOS gate, ii) transmission gate. Implement two input multiplexer using CMOS transmission gate.	3	3	5
C)	Write short note on SR latch circuit.	3	3	5
D)	Write short note pass transistor logic..	3	3	5
Q.4				
A)	Give the classification of semiconductor memories. Draw typical random access memory array organization.	4	3	5
B)	Design a 4-bit X 4-bit NOR based ROM array to store following data stream. Also write its column and rows combination. Data: 1001 1110 0110 1001 Draw layout for circuit designed.	4	3	10
C)	Discuss the operation of resistive-load SRAM Cell.	4	3	5
Q.5				
A)	Discuss the operation of three transistor DRAM Cell.	4	3	10
B)	Explain Partial-product generation.	5	3	5
C)	Write short note on barrel shifter.	5	3	5
Q.6				
A)	What is clock skew? What are the sources of clock skew? How it can be overcome?	6	4	5
B)	Explain clock system architecture.	6	4	5
C)	Explain in detail global clock generator of clock system.	6	4	5
D)	Comment on the advantages and disadvantages of H-trees and clock grids. How does the hybrid tree/grid improve on a standard grid?	6	4	5
Q.7				
A)	Explain how an electrostatic discharge event could cause latchup on a CMOS chip	7	4	5
B)	Define: A) VDD & GND pads. B) Input and Output Pads. C) Bidirectional pads.	7	4	5

	D) Analog pads. Draw bidirectional pad circuitry.			
C)	Write short note on Elmore delay.	7	4	5
D)	Define crosstalk. What are the effect of crosstalk delay and crosstalk noise on interconnect.	7	4	5